

Introduction to Clock Constraints Demo Script

Introduction

This demonstration script provides high-level instructions on how to constrain the clock and perform basic timing analysis in a design using the AMD Vivado™ Design Suite.

Preparation:

- Required files: \$TRAINING_PATH/ClkConstr_Intro/demo/KCU105/verilog
- Required hardware: None
- Supporting materials: None

Clock Creation

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none">• Launch the Vivado Design Suite.• Unzip the project using the Tcl Console: <pre>exec unzip \$::env(TRAINING_PATH) / ClkConstr_Intro/demo/KCU105/veri log.zip -d \$::env(TRAINING_PATH) / ClkConstr_Intro/demo/KCU105/ verilog</pre>	
<ul style="list-style-type: none">• Open the wave_gen.xpr design from the following directory: \$TRAINING_PATH/ClkConstr_Intro/ demo/KCU105/verilog	
<ul style="list-style-type: none">• Open the wave_gen_timing_ClkConstr_Intro.xdc file.	<p>Note that there are no timing constraints entered in the XDC file.</p> <p>You will be entering the clock constraints for the design by using the Constraints Wizard.</p>
<ul style="list-style-type: none">• Open the synthesized design.	
<ul style="list-style-type: none">• Launch the Constraints Wizard from Synthesis > Open Synthesized Design to make the initial clock constraints on the design.	<p>The Constraints Wizard guides you through creating timing constraints. It analyzes the design for missing timing constraints and makes recommendations.</p>

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Open the Constraints Wizard. Click Next in the Welcome page of the Constraints Wizard to identify any missing timing constraints in the design. 	The Constraints Wizard is designed to make it as easy as possible to make complete constraints for any design (hence all the questions). In this case, wave_gen does not need any special timing constraints.
<ul style="list-style-type: none"> Click Existing Create Clock Constraints(1) and see that the clock is already added. 	The Primary Clocks dialog box in the Constraints Wizard identifies the missing primary clocks, if any, in the design, and allows you to enter the period/frequency of the primary clock.
<ul style="list-style-type: none"> Click Skip to Finish after entering the clock constraint. Select the View Timing Constraints option in the Constraints Summary page. Click Finish. 	<p>The Summary window will acknowledge the new clock constraint. The utility will then close without opening the Constraints Editor.</p> <p>The Constraints Editor will then open and show the new clock constraint.</p>
<ul style="list-style-type: none"> Enter report_clocks in the Tcl Console. Make sure to press the <Enter> key. 	<p>Describe the contents of this report.</p> <p>From the Clocks report, what is the input clock to the MMCM?</p> <p>How many output clocks are generated from this MMCM?</p>
<ul style="list-style-type: none"> Open the clk_gen.v file from the Sources window. 	<p>Verify that the signals clk_pin_p, clk_out1, and clk_out2 are made from the clk_core (bottom of file).</p> <p>From this you will see that clk_rx and clk_tx are out1 and out2. This matches the output signal names from the top of the file.</p>
<ul style="list-style-type: none"> Double-click the clk_core.xci file in the Sources window. This will open the Re-customize IP Wizard. Close the Re-customize IP Wizard without saving any changes. 	<p>Review the output frequencies generated by the MMCM.</p> <p>Can you explain how this MMCM was configured to produce clocks of 200 MHz and 193.75 MHz? Hint: Go to the Summary tab.</p>
<ul style="list-style-type: none"> Click Report Clock Networks in the Flow Navigator. 	Review how the report generated confirms how the MMCM made the three output clocks.

Basic Static Timing Analysis

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none"> Click Report Timing Summary to generate a Timing Summary report from the synthesized design. 	<p>Review the following:</p> <ul style="list-style-type: none"> Organization of the report in the GUI Design Timing Summary Check Timing Report Intra-Clock paths Inter-Clock paths User Ignored Paths Unconstrained Paths
<ul style="list-style-type: none"> Select the longest setup path for <code>clk_out1_clk_core</code> under Intra-Clock Paths. 	<p>Review the following:</p> <ul style="list-style-type: none"> Path properties Confirm the slack calculation for hold time (arrival time – required time) Logic descriptions Element delay and cumulative delay Schematic generation and cross probing to source HDL
<ul style="list-style-type: none"> Describe the inter-clock paths and the possible need for synchronization circuits. Select the longest path in the Inter-clock Paths section. 	<p>Review the possible need for synchronization circuits.</p> <p>Review the path to show that they have different clocks on the source and destination flip-flops.</p>
<ul style="list-style-type: none"> Click Report Clock Interaction to generate a Clock Interaction report. 	<p>Review the following:</p> <ul style="list-style-type: none"> Color coding for different type of paths Source clock/destination clock chart Right-click options for the paths between each clock domain.

Action with Description	Point of Emphasis and Key Takeaway
<ul style="list-style-type: none">Facilitate an open-ended discussion on fixing the design.	<p>Review the following:</p> <ul style="list-style-type: none">Synchronization circuitryFixing timing problemsNeed for path-specific constraints <p>If I do all of these things, will I fix all the timing problems?</p> <p>How accurate are these timing numbers?</p> <p>Note: In this demo, all this analysis can be done without having to complete a single implementation (saved huge amount of time).</p>

Summary

This demo illustrated how to create initial clock constraints and verify the clocking structures built into your design using some of the most common reports. It also illustrated the static timing analysis capabilities of the Vivado Design Suite to perform some basic timing verification.

References:

- Supporting materials
 - Vivado Design Suite User Guide (Using Constraints)* (UG903)
 - Vivado Design Suite User Guide (Design Analysis and Closure Techniques)* (UG906)